WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Thursday, January 27, 2005

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L20	l11.clm. and l15	6
☐	L19	l11 and l15	15
☐	L18	l9 and (delay near2 driver) and L15	3
☐	L17	(l9 same driver) and L15	1
☐	L16	l9 and L15	28
☐	L15	l13 or L14	2143
☐	L14	713/401,500,503.ccls.	1099
☐	L13	327/161,237,269,508.ccls.	1062
☐	L12	L11 with (adjust$4 or siz$4)	13
☐	L11	(ic or (integrated adj circuit)) with (clock$4 near5 propagat$4 near5 delay$4)	136
☐	L10	(ic or (integrated adj circuit)) same (clock$4 near5 propagat$4 near5 delay$4 near5 adjust$4)	14
☐	L9	(ic or (integrated adj circuit)) same (clock$4 near5 propagat$4 near5 delay$4)	274
☐	L8	(delay near3 bias$4 near3 (clock$4 or tim$4)) same (modulat$4 near3 (clock$4 or tim$4))	3
☐	L7	L6 and ((output$4 or send$4) near3 delay near3 bias$4 near3 (clock$4 or tim$4))	0
☐	L6	(delay near2 driver) and ((output$4 or send$4) near5 modulat$4 near5 (clock$4 or tim$4))	15
☐	L5	(delay near2 driver) same ((output$4 or send$4) near5 modulat$4 near5 (clock$4 or tim$4))	0
☐	L4	(delay near2 driver) near5 (output$4 or send$4) near5 (modulat$4 near5 (clock$4 or tim$4))	0
☐	L3	(delay near2 driver) near5 (output$4 or send$4) near5 (modulat$4 near2 (clock$4 or tim$4))	0
☐	L2	(delay near2 driver) near5 (siz$4 or adjust$4) near5 ((based or depend$4 or respons$4) near3 (clock$4 or tim$4))	2
☐	L1	(biasable near2 delay near2 driver)	1

END OF SEARCH HISTORY

L18: Entry 1 of 3 File: USPT Jul 2, 2002

DOCUMENT-IDENTIFIER: US 6414530 B2
TITLE: Semiconductor integrated circuit device, semiconductor memory system and clock synchronous circuit

Brief Summary Text (39):
A lattice-like delay circuit is configured wherein a first delay circuit or coarse delay for propagating a clock pulse with relatively low time resolution, a first edge detector and a first multiplexer are used to form or create a clock signal delayed by one clock in association with the relatively low time resolution, a second coarse delay having relatively high time resolution, a second edge detector and a second multiplexer are used to correct an error of the first coarse delay, included in the above signal, and a plurality of logic gate means each of which is provided with impedance means for making coupling between two input signals inputted between first and second input terminals as a second delay circuit having high time resolution as the above second coarse delay and each of which produces an output signal obtained by inverting the input signals, are used so as to be placed in lattice form in first and second signal transfer directions. The lattice-like delay circuit is used wherein the respective logic gate means extending from the first to the last as seen in the first signal transfer direction are respectively successively supplied with input clock signals with their delays as seen in the first signal transfer direction, and output signals are obtained from output terminals of the plurality of logic gate means placed in at least the final stage or the immediately preceding stage as seen in the second signal transfer direction and arranged in the first signal transfer direction. The lattice-like delay circuit referred to above is installed in a semiconductor integrated circuit device such as a synchronous DRAM or the like.

Detailed Description Text (144):
Thus, if tDmax is set so as to meet the expression (10), it is then possible to eliminate the restrictions on the minimum cycle of the synchronizable clock. However, the number of clock cycles required to generate the synchronizing clock increases with an increase in n. Namely, although three clock cycles were required for synchronization even at the lowest because of measurements of two clock cycles in total: one cycle in the case of the coarse delay CD1 and one cycle in the case of the lattice-like delay circuit SQUAD1, the number of clock cycles increases to the two clock cycles or more. In order to limit the number of the clock cycles low in reverse, it is necessary that a delay d11 of the internal clock driver DRV1 and a delay d10 of the clock receiver RCV1 are reduced so that the delay times dDM1 and dDM2 of the dummy delay circuits DMDL1 and DMDL2 are diminished.

Current US Original Classification (1):
327/269

L10: Entry 4 of 14 File: USPT Dec 26, 2000

DOCUMENT-IDENTIFIER: US 6166990 A

**** See image for Certificate of Correction ****

TITLE: Clock reproduction circuit that can reproduce internal clock signal correctly in synchronization with external clock signal

CLAIMS:

27. The synchronous semiconductor integrated circuit device according to claim 23, wherein said coarse adjust circuit includes a delay monitor for compensating for a difference in signal propagation delay between the internal clock signal and the base clock signal.

L10: Entry 5 of 14 File: USPT Feb 10, 1998

DOCUMENT-IDENTIFIER: US 5717729 A
TITLE: Low skew remote absolute delay regulator chip

Brief Summary Text (10):
An example of a prior art technique used to reduce PVTL-caused clock skew is disclosed in an article titled, CLOCK BUFFER CHIP WITH ABSOLUTE DELAY REGULATION OVER PROCESS AND ENVIRONMENTAL VARIATIONS, by Watson et al., from 1992 IEEE Custom Integrated Circuit Conference. Here, a delay regulator circuit of a clock repeater chip located on a computer module performs a precise measurement of the propagation delay of a clock signal processed by the repeater chip and adjusts that delay to a standard value prior to distributing the processed clock signal to other IC chips on the module. Each repeater chip provides an interface between a globally-distributed (system) input clock signal and corresponding locally-distributed (module) output clock signals. By adjusting the delay in the chip, a fixed-phase relationship is maintained between the input and output clock signals.

L10: Entry 6 of 14 File: USPT Nov 29, 1994

DOCUMENT-IDENTIFIER: US 5369640 A
TITLE: Method and apparatus for clock skew reduction through remote delay regulation

Brief Summary Text (9):
An example of a technique used to reduce PVTL-caused clock skew is disclosed in an article titled, CLOCK BUFFER CHIP WITH ABSOLUTE DELAY REGULATION OVER PROCESS AND ENVIRONMENTAL VARIATIONS, by Watson et al., from 1992 IEEE Custom Integrated Circuit Conference. Here, a delay regulator circuit of a clock repeater chip located on a computer module performs a precise measurement of the propagation delay of clock signal processed by the repeater chip and adjusts that delay to a standard value prior to distributing the processed clock signal to other IC chips on the module. Each repeater chip provides an interface between a globally-distributed (system) input clock signal and corresponding locally-distributed (module) output clock signals. By adjusting the delay in the chip, a fixed-phase relationship is maintained between the input and output clock signals.

Brief Summary Text (20):
The present invention resides in a method and apparatus for measuring the effects of intrinsic propagation delay experienced by a system clock signal propagating through an extended clock distribution path that encompasses a clock repeater chip, a module transmission network and a clock distribution network of an associated integrated circuit (IC) chip. A remote delay regulator circuit measures the effects of the intrinsic propagation delay and adjusts the system clock signal so as to deliver a low-skew clock signal to the point-of-use on the associated IC chip. Delay adjustment is provided by adding sufficient controlled amounts of delay, i.e., insertion delay, to the system clock signal, thereby maintaining a fixed-phase relationship among all clock signals distributed by a central clock module of a computer system at the points where they interact with a system bus. This effective reduction in clock skew permits a significant increase in the effective speed of the bus.

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L10: Entry 7 of 14 File: USPT Nov 23, 1993

DOCUMENT-IDENTIFIER: US 5264746 A
TITLE: Logic circuit board with a clock observation circuit

Abstract Text (1):
This logic circuit board with a clock observation circuit comprises a plurality of logic circuit IC chips and a clock supply IC chip to supply clock signal to such logic circuit IC chips mounted on a printed wiring board. The logic circuit IC chips are respectively connected to the clock supply IC chip via clock supply wires to propagate clock signal, all of which have the same length. Each of the logic circuit IC chips is provided with an observation terminal for clock signal observation, and the clock supply IC chip is provided with an external terminal for clock signal observation. Propagation time adjustment means comprising a delay circuit for adjustment of clock signal propagation time is provided between the clock supply IC chip and the external terminal. Then, the delay in propagation of clock signal is adjusted so that the phase shift of the clock signal observed at the external terminal is the central shift value between the maximum and the minimum shifts of the clock signal observed at the observation terminals of the logic circuit IC chips.

Brief Summary Text (11):
According to another preferred embodiment, the external terminal is disposed on the border of the printed wiring board. More preferably, the propagation time adjustment means adjusts the delay in propagation time for clock signal so that the phase shift of the clock signal observed at the external terminal is identical to the central value of the maximum and the minimum phase shifts in the clock signal observed at the observation terminals of the logic circuit IC chips.

Detailed Description Text (8):
Here, the delay in propagation time from the clock supply IC 13 set at the propagation time adjustment means 18 is arranged so that the propagation delay time for the observation terminals 14A to 14E of the logic circuit IC chips 12A to 12E receiving supplied clock signal is almost the same as that for the external terminal 19.

CLAIMS:

3. A logic circuit board with a clock observation circuit of claim 1, wherein said propagation time adjustment means adjusts the delay in propagation time for said clock signal so that the phase shift of the clock signal observed at said external terminal is identical to the central value of the maximum and the minimum phase shifts in the clock signal observed at the observation terminals of the logic circuit IC chips.

Previous Doc Next Doc Go to Doc#

L10: Entry 8 of 14 File: USPT Jul 5, 1988

DOCUMENT-IDENTIFIER: US 4755704 A

**** See image for Certificate of Correction ****

TITLE: Automatic clock de-skewing apparatus

Brief Summary Text (18):

In a particular preferred embodiment of the invention, a data processing system is constructed and arranged such that each of a plurality of its circuit boards includes a clock distribution integrated circuit chip responsive to a main-system clock for providing clock signals for distribution to other circuitry provided on its respective board. Each clock distribution chip includes automatic clock de-skewing circuitry for automatically adjusting the propagation delay of the clock distribution chip so that the output clock signals provided to circuitry on its respective board have an accurate predetermined relationship relative to the main-system clock. The automatic de-skewing circuitry provided on each clock distribution chip employs an accurate, relative large reference delay element which is advantageously provided by a specially formed conductor incorporated in the board containing the clock distribution chip.

L2: Entry 1 of 2 File: USPT Mar 28, 2000

DOCUMENT-IDENTIFIER: US 6043694 A
TITLE: Lock arrangement for a calibrated DLL in DDR SDRAM applications

CLAIMS:

1. A calibrated Delay Locked Loop (DLL) comprising:

a DLL locking arrangement comprising a selectively adjustable delay line which is responsive to a received clock input signal for generating an output clock signal that is in phase with the clock input signal, and a driver for providing an output data signal from the calibrated Delay Locked Loop; and

a gating circuit coupled between the selectively adjustable delay line and the driver and being responsive to the output clock signal from the selectively adjustable delay line for separately (a) generating an imitation data signal which is in phase with said output clock signal from the selectively adjustable delay line, and (b) latching a received input data signal to generate a data output signal that is in phase with said output clock signal from the selectively adjustable delay line, the gating circuit being further responsive to a switching control signal having a first logical value for coupling only the data output signal generated within the gating circuit to an input of the driver, and to the switching control signal having a second logical value for only coupling the imitation data signal generated within the gating circuit to the input of the driver; and

wherein the DLL locking arrangement is responsive to the switching control signal having the second logical value for synchronizing the imitation data signal appearing at the driver output to the clock input signal received by the DLL locking arrangement to generate the output clock signal from the adjustable delay line, and is responsive to the switching control signal having the first logical value to disable any synchronization of the output data signal at the driver output to the clock input signal and to maintain a latest output clock signal produced by the adjustable delay line during the period when the switching control signal having the second logical value was applied.

10. A calibrated Delay Locked Loop (DLL) arrangement comprising:

a selectively adjustable delay line responsive to a clock input signal for generating an output clock signal having a selectively adjustable delay;

a gating circuit coupled between the selectively adjustable delay line and a driver and being responsive to the output clock signal from the selectively adjustable delay line for separately (a) generating an imitation data signal which is in phase with said output clock signal, and (b) latching a received input data signal to generate a data output signal that is in phase with said output clock signal from the selectively adjustable delay line, the gating circuit being further responsive to a switching control signal having a first logical value for coupling only the data output signal to an input of the driver, and to the switching control signal having a second logical value for only coupling the imitation data signal to the input of the driver;

the driver is responsive to the gating circuit for generating an output of the calibrated DLL arrangement; and

a phase comparator responsive to the switching control signal having the second logical value for comparing the clock input signal with the imitation data signal appearing at the driver output and generating a control signal representative of the comparison to the adjustable delay line for causing the output clock signal therefrom to be selectively placed in phase with the input clock signal, and responsive to the switching control signal having the first logical value to disable any comparison of the clock input signal with the data output signal at the driver output and maintain a latest adjustable delay introduced by the delay line during the period when the switching control signal having the second logical value was applied to the phase comparator.

14. A calibrated Delay Locked Loop arrangement comprising:

a receiver for receiving a clock input signal and for generating a clock output signal corresponding to the clock input signal;

a selectively adjustable delay line responsive to the clock output signal from the receiver for generating an output clock signal having a selectively adjustable delay therein;

a gating circuit coupled between the selectively adjustable delay line and a driver and being responsive to the output clock signal from the selectively adjustable delay line for separately (a) generating an imitation data signal which is in phase with said output clock signal, and (b) latching a received input data signal to generate a data output signal that is in phase with said output clock signal from the selectively adjustable delay line, the gating circuit being further responsive to a switching control signal having a first logical value for coupling only the data output signal to an output thereof, and to the switching control signal having a second logical value for only coupling the imitation data signal to the output thereof;

the driver providing an output signal for the calibrated Delay Locked Loop arrangement; and

a feedback loop coupled to an output of the driver comprising a phase comparator which is responsive to the switching control signal having the second logical value for comparing the clock input signal with the driver output signal and generating a control signal to the adjustable delay line for selectively introducing a corresponding delay into the output clock signal from the adjustable delay line, and being responsive to the switching control signal having the first logical value to prevent the comparison of the clock input signal with the driver output signal and maintain a latest adjustable delay introduced by the delay line.

Previous Doc Next Doc Go to Doc#

L10: Entry 2 of 14 File: USPT Dec 16, 2003

DOCUMENT-IDENTIFIER: US 6665219 B2
TITLE: Method of reducing standby current during power down mode

CLAIMS:

4. An integrated circuit memory device comprising: a clock signal medium adapted to conduct a periodic clock signal from a clock signal input node to a first termination node during a first power down time interval and from said clock signal input node past said first termination node to a second termination node during a second power up time interval, said clock signal medium including a delay device between said first and second termination nodes, said delay device adapted to adjust a propagation delay of said periodic clock signal over said portion of said clock signal medium between said first and second termination nodes, said delay device dissipating a first quantity of heat during said first power down time interval and a second larger quantity of heat during said second power up time interval.

L10: Entry 3 of 14 File: USPT Sep 2, 2003

DOCUMENT-IDENTIFIER: US 6615204 B1
TITLE: Method and system for hybrid mapping of objects into a relational data base to provide high-speed performance and update flexibility

Abstract Text (1):
A clock edge placement circuit for implementing source synchronous communication between integrated circuit devices. The clock edge placement circuit includes a delay line having an input to receive a clock signal from an external clock source. A corresponding output is included to provide the clock signal to external logic elements. The delay line structure adapted to add a propagation delay to the input, wherein the propagation delay is sized such that the phase of the clock signal is adjusted to control synchronous sampling by the external logic elements. The delay line is adapted to dynamically adjust the delay such that the phase of the clock signal at the output remains adjusted to control synchronous sampling by the external logic as variables affecting the phase of the clock signal change over time. A series of taps are included within the delay line. The delay line uses the series of taps to add a variable delay for adjusting the phase of the clock signal. Each tap is configured to add an incremental delay to the input to generate the variable delay.

L10: Entry 1 of 14 File: USPT Jan 20, 2004

DOCUMENT-IDENTIFIER: US 6680636 B1

**** See image for Certificate of Correction ****

TITLE: Method and system for clock cycle measurement and delay offset

Abstract Text (1):
A clock edge placement circuit for implementing source synchronous communication between integrated circuit devices. The clock edge placement circuit includes a delay line having an input to receive a clock signal from an external clock source. A corresponding output is included to provide the clock signal to external logic elements. The delay line structure adapted to add a propagation delay to the input, wherein the propagation delay is sized such that the phase of the clock signal is adjusted to control synchronous sampling by the external logic elements. The delay line is adapted to dynamically adjust the delay such that the phase of the clock signal at the output remains adjusted to control synchronous sampling by the external logic as variables affecting the phase of the clock signal change over time. A series of taps are included within the delay line. The delay line uses the series of taps to add a variable delay for adjusting the phase of the clock signal. Each tap is configured to add an incremental delay to the input to generate the variable delay.

Brief Summary Text (18):
In one embodiment, the present invention comprises a clock edge placement circuit for implementing source synchronous communication between integrated circuit devices. The clock edge placement circuit includes a delay line having an input to receive a clock signal from an external clock source. A corresponding output is included to provide the clock signal to external logic elements. The delay line is adapted to add a propagation delay to the input, wherein the propagation delay is sized such that the phase of the clock signal is adjusted to control synchronous sampling by the external logic elements. The delay line is configured to allow the dynamic adjustment of the propagation delay such that the phase of the clock signal at the output remains adjusted to control synchronous sampling by the external logic as variables affecting the phase of the clock signal change over time. A plurality of taps are included within the delay line, wherein each tap his configured to add an incremental delay to the input to generate the variable delay.

Detailed Description Text (10):
The system of the present invention functions by adjusting the propagation delay of the clock channel (e.g., clock channel 37 of FIG. 3) between the source chip 31 and the destination chip 32 to eliminate the clock skew distortion limitations of prior art source synchronous multichip device implementations. The present invention accurately and reliably places the rising edge of the clock signal at the optimal setup and hold times for the data signal, as shown in FIG. 5. Thus, instead of, for example, distributing a common clock signal in parallel to the source and destination chips 31 and 32, the clock signal is transmitted directly, along with the data, from the source chip 31 to the destination chip 32 with the assurance that the clock edge placement circuit (e.g., circuit 60 shown in FIG. 6 below) will adjust the phase of the clock signal in accordance with setup-and-hold times to maintain reliable synchronous sampling. This aspect allows integrated circuit devices in accordance with the present invention to realize higher clock speeds for

L8: Entry 2 of 3 File: USPT Jun 5, 1973

DOCUMENT-IDENTIFIER: US 3737900 A
TITLE: DIGITAL DOPPLER PROCESSOR

Detailed Description Text (78):
when .DELTA.R(n) exceeds a range resolution increment (corresponding to the range-gated interval of each range bin) during the doppler processing interval N/PRF, then the value A.sub.ni of the range gated video (for a given range bin) could be taken from the preceeding range bin for the remainder of the doppler processing interval. Such range registration function may be mechanized by means of a computing element 62 (in FIG. 9) cooperating to selectively control a shift register (not shown) in which each range-gated single successive range-trace signal is temporarily stored. Alternatively, a time modulator 58 or otherr voltage controlled delay may be interposed at the trigger input to the range-gated means 40 of FIG. 3. In this way, a preselected delay or time bias (T.sub.o) may be selectively reduced (T.sub.o - .DELTA. t), whereby a given range-gated interval or range bin represents a correspondingly lesser range.

L8: Entry 1 of 3 File: USPT Jun 16, 1998

DOCUMENT-IDENTIFIER: US 5768449 A
TITLE: Optical transmission system and optical transmission method

Brief Summary Text (57):
the levels P.sub.1 and P.sub.2 of the first and second modulation signals, the time delay quantity in the delay portion and the bias voltage supplied with the external light modulation portion are set so that a difference DL.sub.x between the delay quantities DL.sub.1 and DL.sub.2, that is DL.sub.x =(DL.sub.2 -DL.sub.1), the "m" and coefficients of input/output transfer functions F.sub.1 (x) and F.sub.2 (x) satisfy the relation expressed as follows:

Brief Summary Text (58):
According to the sixth aspect, as hereinabove described, the delay quantities DL.sub.1 and DL.sub.2 of the transmission paths for the first and second modulation signals are different from each other. In this case, it is possible to reduce the tertiary distortion included in the light signal by setting the levels P.sub.1 and P.sub.2 of the first and second modulation signals, the time delay quantity in the delay portion and the bias voltage applied to the external light modulation portion at proper values so that the difference DL.sub.x =(DL.sub.2 -DL.sub.1) between the delay quantities DL.sub.1 and DL.sub.2, the "m" and the coefficients of the input/output transfer functions F.sub.1 (x) and F.sub.2 (x) satisfy the relation expressed as follows:

Brief Summary Text (65):
the levels P.sub.1 and P.sub.2 of the first and second modulation signals, the time delay quantity in the delay portion and the bias voltage supplied with the external light modulation portion are set so that the difference DL.sub.x between the delay quantities DL.sub.1 and DL.sub.2, that is DL.sub.x =(DL.sub.2 -DL.sub.1) the "m" and coefficients of input/output transfer functions F.sub.1 (x) and F.sub.2 (x) satisfy the relation expressed as follows:

Brief Summary Text (67):
In this case, it is possible to reduce the tertiary distortion included in the light signal by setting the levels P.sub.1 and P.sub.2 of the first and second modulation signals, the time delay quantity in the delay portion and the bias voltage supplied with the external light modulation portion at proper values so that the "m" and the coefficients of the input/output transfer functions F.sub.1 (x) and F.sub.2 (x) satisfy the relation expressed as follows:

Brief Summary Text (89):
the levels P.sub.1 and P.sub.2 of the first and second modulation signals, the time delay quantity in the delay portion and the bias voltage supplied with the external light modulation portion are set so that the difference DL.sub.x between the delay quantities DL.sub.1 and DL.sub.2, that is DL.sub.x =(DL.sub.2 -DL.sub.1), the "m" and coefficients of the input/output transfer functions F.sub.1 (x) and F.sub.2 (x) satisfy the relation expressed as follows:

Brief Summary Text (90):
According to the tenth aspect, as hereinabove described, the delay quantities DL.sub.1 and DL.sub.2 of the transmission paths for the first and second modulation